

AMKASYN
Adapter AP-CI4 (Part-No. O778)
ACC – SubD 9pin
(ACC – CANopen)

Version: 2009/28.0 Part-No.: 201550





Notes on this document

Name:	PDK	201550	Adapter	AP-CI4	en

Version:

Version	Change	Letter symbol
2009/28.0	Pin Assignment; Correction	Bls

Product version:

Device Firmware Version Hardware Version

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Type plate data for each unit

Software version

Device configuration and application

Type of fault/problem and suspected cause

• Diagnostic messages (error messages)

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1 Intended Use



picture name: ZCH_Adapter-AP-CI4

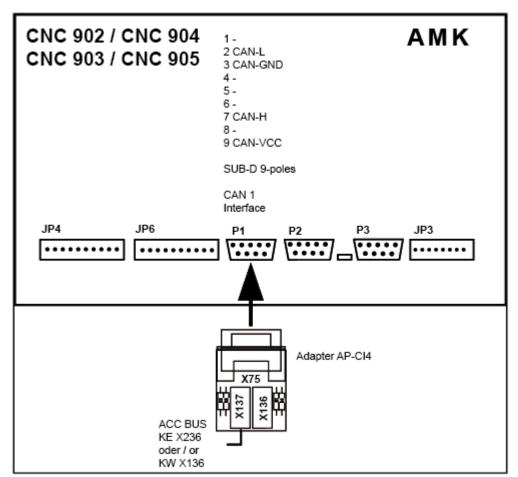
The adapter AP-CI4 interlinks the ACC bus interface (AMK CAN Communication) of the AMK devices with a higher level controller.

The ACC bus interface is located on the top of the AMK controller cards for KW and KWD modules or rather on the top of the KE module.



2 Application examples

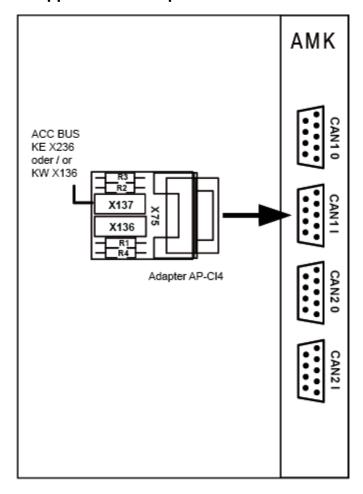
2.1 Application example AMK CNC900 Controller, compact module line 902, 903, 904, 905 Without hardware synchronization signal



picture name: ZCH_AP-CI4_CNC900



2.2 Application example AMK CNC900 Controller with hardware synchronization signal



picture name: ZCH_AP-CI4_CNC900_e



A terminating connector will be not used. The termination connector is inside the CNC900 controller. Higher level controller who support the hardware synchronization signal has to complete with two 00hm resistances (R1 and R2) at the adapter AP-CI4. The interlink from adapter AP-CI4 to the ACC bus must be at first or last ACC node. The adapter AP-CI4 is only allowed to connect to a ACC bus at zero current.



3 Pin Assignment

Pin SUB-D-9 socket	Signal	IEEE1394	X136 ACC-IN	X137 ACC-OUT
1		1	Opt.GND	Opt.GND
2	CAN_L	2	GND	GND
3	GND	3	SYNC_H	CAN_H
4	(*SYNC_L)	4	SYNC_L	CAN_L
5		5	CAN_H	SYNC_H
6		6	CAN_L	SYNC_L
7	CAN_H			
8	(*SYNC_H)			
9				

^{*}only higher level controller with hardware synchronization signal



4 EMC Notes

The ACC bus which is connected, must have shielded cables. The shield must have a conducting connection to the connector housing.



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